

CLAIMS

What is claimed is:

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1. A system comprising:
 - a system memory controller; and
 - a first memory module comprising:
 - a first memory module controller coupled to the system memory controller; and
 - a first plurality of memory devices coupled to the first memory module controller.
 2. The system of claim 1, further comprising a first memory bus coupled between the system first memory module and the first memory module controller.
 3. The system of claim 2, wherein the first memory bus comprises a clock signal.
 4. The system of claim 2, wherein the first memory bus comprises a handshake signal that indicates when the first memory module controller is communicating data to the system memory controller.
 5. The system of claim 2, further comprising a second memory bus coupled between first memory module controller and the first plurality of memory devices.
 6. The system of claim 5, wherein the second memory bus comprises a clock signal.

1 7. The system of claim 5, wherein the first memory bus operates at a first
2 data rate and the second memory bus operates at a second data rate, wherein
3 the first data rate is different than the second data rate.

1 8. The system of claim 5, wherein the first memory bus has a first number
2 of signal lines and the second memory bus has a second number of signal
3 lines, wherein the first number of signal lines is different than the second
4 number of signal lines.

1 9. The system of claim 5, wherein the first memory module controller
2 comprises:
3 request handling circuitry structured to receive a first memory
4 transaction from the first memory bus; and
5 control logic coupled to the request handling circuitry and generating a
6 second memory transaction on the second memory bus corresponding to the
7 first memory transaction on the first bus.

1 10. The system of claim 2, wherein the first memory bus carries time-
2 multiplexed data and address information, and the second memory bus
3 includes separate address and data lines.

1 11. The system of claim 1, wherein the first memory module is a dual in-
2 line first memory module (DIMM).

1 12. The system of claim 1, wherein the first memory module is a single in-
2 line first memory module (SIMM).

1 13. The system of claim 1, wherein the first plurality of memory devices
2 comprise volatile memory devices.

1 14. The system of claim 1, wherein the first plurality of memory devices
2 comprise nonvolatile memory devices.

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As 1 15. The system of claim 1, further comprising a second memory module
2 comprising:

3 a second memory module controller coupled to the system
4 memory controller; and

5 a second plurality of memory devices coupled to the second
6 memory module controller.

1 16. The system of claim 15, wherein the first plurality of memory devices
2 stores data in a different way than the second plurality of memory devices.

1 17. A system comprising:

2 a system memory controller;

3 a memory bus coupled to the system memory controller; and

4 a memory comprising:

5 a memory module controller coupled to the memory bus; and

6 a plurality of memory devices coupled to the memory module

7 controller, wherein the memory module controller receives a first memory
8 transaction from the memory bus in a first format and provides a second
9 memory transaction in a second format to at least one of the second plurality
10 of memory devices.

1 18. A method of communicating a memory transaction between a system
2 memory controller and at least one of a plurality of memory devices on a
3 memory module including a memory module controller, the method
4 comprising the steps of:

5 sending a memory transaction from the system memory controller to
6 the memory module controller, the memory transaction having a first
7 format;
8 reformatting the memory transaction for the at least one of the
9 memory devices; and
10 sending the reformatted memory transaction to the at least one of the
11 memory devices.

1 19. The method of claim 18, wherein the memory transaction is a read
2 transaction.

1 20. The method of claim 18, wherein the memory transaction is a write
2 transaction.

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